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(54) Process for bonding and electrically connecting microsystems integrated in several distinct substrates

(57) A process for bonding two distinct substrates that integrate microsystems, comprising the steps of: making micro-integrated devices in at least one of the two substrates using microelectronic processing techniques; and bonding said substrates. The bonding is performed by making on a first substrate (33) bonding regions (32) of deformable material and by pressing said substrates one against another so as to deform the bonding regions and to cause them to react chemically with the second substrate (34). The bonding regions are preferably formed by a thick layer (30) made of a material chosen from among aluminium, copper and nickel, covered by a thin layer (31) made of a material chosen from between palladium and platinum. Spacing regions (25') guarantee exact spacing between the two wafers.

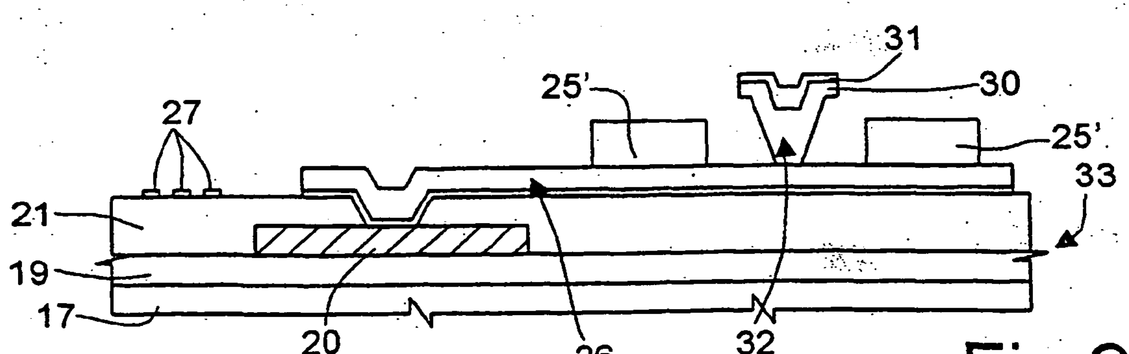

Fig.9

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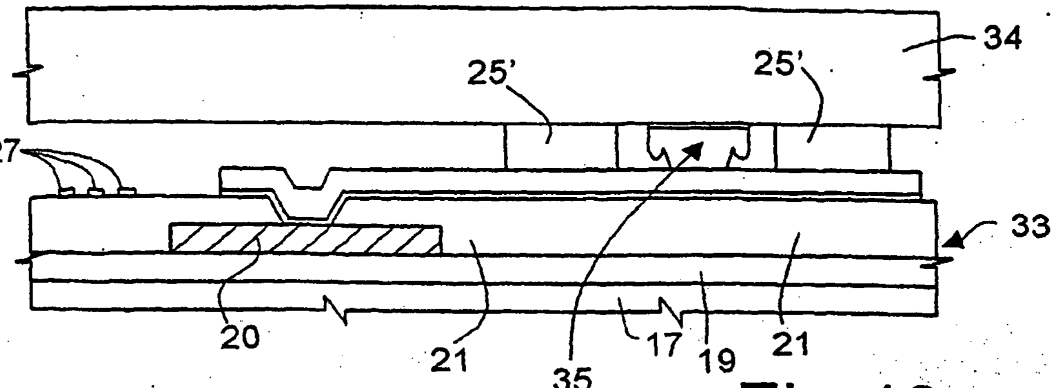

Fig. 10

Description

[0001] The present invention relates to a process for bonding and electrically connecting microsystems integrated in several distinct substrates.

[0002] As is known, numerous technological approaches allow manufacturing integrated circuits wherein the electronic circuitry coexists with a sensor element or an actuator (micro-electromechanical device). The traditional approaches envisage the production of the sensors/actuators and circuitry in a same silicon substrate (surface and epitaxial sensors). The most recent approaches envisage, instead, several substrates and the electronic circuit, the micro-electromechanical device or parts thereof are formed in distinct wafers that are subsequently bonded together and finally diced.

[0003] Bonding of the wafers is obtained by causing one or more metals to react with one another, with the silicon of one of the substrates or with metal alloys. To this aim, one or more metals are deposited in sequence on the surface of one or both of the wafers. Then the surfaces to be bonded are brought into intimate contact through a piston that applies a predetermined pressure, as shown in Figure 1, which illustrates a substrate 1, a first wafer 2, a layer of bonding material 3, a second wafer 4, and a piston 5 which presses the second wafer 4 against the first wafer 2.

[0004] Under the pressure of the piston 4, the bonding material reacts only where the surfaces are in a mechanical contact, and the areas that are not in contact are not bonded.

[0005] With this solution, bonding between the wafers depends to a large extent upon the mechanical force of the piston; in particular, criticalities are linked, on the one hand, to the uniformity of pressure applied by the piston and, on the other, to the possible presence of foreign bodies.

[0006] In particular, for example in the presence of non-planar areas, the pressure applied by the piston may be non-uniform over the entire surface or over the entire area where bonding is to be obtained. In this case, the presence of areas of the two wafers that are not in contact prevents bonding of these areas.

[0007] In addition, the presence of particles, acting as spacers, also entails absence of contact, which prevents bonding, as shown, by way of example, in Figure 1, wherein a particle 7 prevents bonding in an area of the surfaces of the wafers 2, 4.

[0008] On the other hand, application of excessive pressure in an attempt to achieve uniform contact in the areas to be bonded may be counterproductive. In fact the deformation of the substrate thus induced causes stresses in the material that persist over time, weakening the bonding joints and/or subsequently causing undesired deformations, in particular in case of suspended structures. For example, a mobile part (such as a rotor of a micro-actuator), once it is released, tends to relieve the accumulated stresses. In this case, the mobile part may get deformed and undergo an undesired spatial displacement, such as might impair proper operation of the structure or, in any case, reduce efficiency thereof.

[0009] The aim of the present invention is to provide a manufacturing process allowing a good bonding quality to be achieved between wafers of semiconductor material.

[0010] According to the present invention there are provided a process for bonding distinct substrates, as well as a device obtained thereby, as defined in Claims 1 and 8, respectively.

[0011] For a better understanding of the present invention, preferred embodiments thereof are now described, purely by way of nonlimiting example, with reference to the attached drawings, wherein:

- Figure 1 shows the bonding of two wafers according to the prior art;
- Figure 2 illustrates a cross-section of two bonded wafers, according to one aspect of the invention;
- Figures 3-10 show, at an enlarged scale, successive steps of the process for bonding two wafers of semiconductor material, according to the invention;
- Figures 11 and 12 show two steps for bonding two wafers of semiconductor material, in a non-planar surface area; and
- Figure 13 shows a cross-section of a device formed in two bonded substrates, in a different embodiment of the invention.

[0012] The invention is based upon the use of a material having characteristics allowing good-quality bonding of two substrates (namely, two wafers of semiconductor material in which electronic devices and/or micro-electromechanical structures are integrated), even in presence of non-planar areas and/or undesired particles acting as spacers, as generally happens in the case of substrates that have undergone previous fabrication processes.

[0013] According to one aspect of the invention, on one of two substrates a layer (possibly a composite layer) is formed having characteristics of high deformability (soft material) and capacity for reaction with the other substrate (bonding material).

[0014] In what follows, the term "soft material" or "deformable material" refers to a material which at standard bonding pressures and at a low temperature (of less than 450-500°C, usable in the final fabrication steps) undergoes deformation without causing stresses on the substrates (for example, a material that has a modulus of elasticity of less than one tenth that of silicon).

[0015] According to another aspect of the invention, as shown in Figure 2, on the first substrate (first wafer 10) there is deposited and possibly defined a stack of layers comprising at least one soft layer 11, of a material having good plastic characteristics and low cost (such as aluminium, copper or nickel), and at least one bond-

ing layer 12, which reacts with the material present on the surface of the second substrate (second wafer 13), forming a eutectic or a silicide. A suitable material is, for example, palladium or platinum.

[0016] According to yet another aspect of the invention, between the soft layer 11 and the bonding layer 12 a diffusion barrier layer 14 may extend, with the dual function of enabling good adhesion between the soft layer 11 and the bonding layer 12 and of constituting a barrier against the diffusion of the various materials of the soft layer 11 and bonding layer 12. A suitable material is, for instance, chromium or titanium.

[0017] Typically, the material of the bonding layer 12 has a high cost, such as to require minimization of its use, adopting low thicknesses.

[0018] In order to carry out bonding, the first wafer 10 and second wafer 13 are brought into mechanical contact with one another. A temperature cycle (for example, at 400°C) and mechanical pressure (through a piston similar to the piston 5 of Figure 1) is carried out so as to cause the bonding layer 12 and the second wafer 13 to react and bond. In this step, the soft layer 11 undergoes deformation and adapts to the existing geometry, compensating for any non-planar regions and/or for the presence of foreign bodies. In practice, the soft layer 11, which has a low cost and hence can be deposited with a large thickness. behaves like a cushion and enables a more even distribution of the pressure exerted by the piston, in such a way as to obtain uniform mechanical contact over the entire area to be bonded and in such a way that any foreign bodies are completely surrounded and embedded in said layer.

[0019] Hereinafter tehre will be described an example of a sequence of steps of a process for bonding and electrically connecting two wafers, one of which houses electrical circuits and the other houses a micro-electromechanical device.

[0020] With reference to Figure 3, first electrical components 18 are formed, in a known way, in a body 17 of semiconductor material. On top of the body 17 various insulating layers -illustrated, for simplicity, as a single insulating layer 19-and various conductive layers, including polycrystalline-silicon regions and various metal levels (not shown in detail) are formed and defined. On top of the insulating layer 19 a top metallization layer, for example of aluminium, is formed and defined, thereby forming a contact region 20, connected to the electrical components 18, as schematically shown in Figure 3. Then a protection layer 21, preferably of silicon dioxide, is deposited and opened, so as to form an opening above the contact region 20.

[0021] Next (Figure 4), a first and a second conductive layers 23, 24 are deposited in succession. For example, the first conductive layer 23 may be of tantalum/aluminium, and the second conductive layer 24 may be of aluminium. Then (Figure 5), a spacing layer 25, for example of silicon dioxide, is deposited.

[0022] Next (Figure 6), the spacing layer 25 is defined so as to form spacing regions 25', and (Figure 7) first the second conductive layer 24 and then the first conductive layer 23 are defined.

[0023] Thus, connection lines 26 are formed by the overlaid first and second conductive layers 23, 24, and stator electrodes 27 formed by the first conductive layer 23 alone.

[0024] Next (Figure 8), a sacrificial layer 28, for example of polyimide, is deposited and opened where the bonding regions are to be formed. As shown in Figure 9, a soft layer 30 (for example of aluminium) and a bonding layer 31 (for example of palladium) are deposited and defined, thus forming bonding regions 32 that extend in part on top of the sacrificial layer 28. In particular, the thickness of the soft layer 30 (which determines, to a first approximation, the thickness of the bonding regions 32) is greater than the thickness of the spacing layer 25. The bonding regions 32 are thus deeper than the spacing regions 25'. Subsequently, the sacrificial layer 28 is removed, and finally (Figure 10) the wafer 33 thus obtained is bonded to a second wafer 34 in which micromechanical structures (not shown) have been formed.

[0025] In this step, the wafers 33, 34 are pressed against one another at a low temperature (for instance, at about 400°C). Consequently, the aluminium of the soft layer 30, which melts at 600°C, softens and spreads out, thus enabling the second wafer 34 to abut against the spacing regions 25', which thus ensure proper spacing between the wafers 33, 34, while the bonding layer 31 reacts with the second wafer 34 to form a silicide or a eutectic, ensuring bonding of the wafers. Then bonding joints 35 are formed, that buckle with respect to the bonding regions 32. The spacing regions 25' may moreover be shaped in such a way as to surround the bonding joints 35 and isolate them from the outside environment.

[0026] By making the bonding regions 32 of an appropriate depth, equal to at least the sum of the depth of the spacing regions 25' and the possible depressions in the second wafer 34, it is possible to ensure bonding even in the non-planar areas of the wafers 33, 34, as shown in Figures 11 and 12, wherein the second wafer 34 has a central depression which would prevent bonding thereof to the first wafer 33. As shown in Figure 12, the central bonding region 32 is deformed less than the lateral regions, but ensures bonding even so.

[0027] Finally, the final fabrication steps are performed, which include, if so envisaged, thinning-out of the first wafer 33 and/or second wafer 34, freeing of the suspended structures, dicing, packaging, etc.

[0028] In certain applications, it may be necessary to have two or more bonding regions 32 arranged in parallel, so as to obtain a section with adequate contact. In fact, to ensure a sufficient deformability of the bonding regions 32, the portion of soft material cannot have an excessive width, i.e., a width greater than a certain value, which can be determined experimentally. In this

case, it is possible to arrange a plurality of bonding joints 35 in parallel. For example, as shown in Figure 13, two bonding joints 35 are connected to a same connection line 26 on the first wafer 33 and to a same conductive region 36 in the second wafer 34. The conductive region 36 is electrically insulated from the remainder of the second wafer 34 by insulating regions 37.

[0029] Figure 13 also shows two spacing regions 25" which do not surround bonding joints 35 and are formed at regions removed from the second wafer 34. In this case, the spacing regions 25" have a function of mechanical support to the second wafer, wherein a linear electrostatic motor is formed, in order to prevent collapse of the suspended regions. Here, the spacing regions 25" are arranged in the proximity of a "spring" 40 which connects a fixed region 41 of the second wafer 34 (which houses the conductive region 36) to a mobile region ("rotor") 42 provided with mobile electrodes 43. The spacing regions 25" face a removed portion that surrounded the spring 40. Possibly further spacing regions 25" having the function of temporary mechanical suspension may be provided also at the suspended regions and must be removed after the bonding step.

[0030] Finally, it is clear that numerous modifications and variations may be made to the process and device described herein, without thereby departing from the scope of the present invention.

[0031] In particular, the invention may be applied to integrated devices of any type formed in at least two substrates.

[0032] The material of the bonding regions may vary. The diffusion barrier material may be present or not, according to the materials used and to the requirements. The soft layer may be modified in terms of hardness, for example by adding copper to the aluminium. Alternatively, the soft layer may be made entirely of copper, possibly coated with a thin layer of platinum, which forms the bonding layer. The soft material may be nickel protected by a very thin layer of palladium, which is exhausted during bonding and enables the formation of a nickel silicide; in this case, then, the nickel layer works both as a soft material, which undergoes deformation and enables adaptation of the bonding joints to the existing geometry, and as a bonding material, which ensures mechanical connection between the two wafers.

[0033] Obviously, the same process can be used to bond three or more wafers together.

Claims

1. A process for bonding two distinct substrates integrating electronic and/or micro-electromechanical devices, comprising the steps of:

   forming micro-integrated devices in at least one of two substrates (10, 13; 33, 34), using microelectronic processing techniques; and

   bonding said substrates;

   characterized in that said step of bonding comprises:

   forming, on a first (10; 33) of said substrates, bonding structures (11, 12, 14; 32) of deformable material; and
   pressing said substrates against each other so as to deform said bonding structures and cause said bonding structures to react chemically with a second substrate (13, 34).

2. The process according to Claim 1, wherein said bonding structures comprise a stack of layers including a soft layer (11) and a bonding layer (12).

3. The process according to Claim 2, further comprising a diffusion barrier layer (14) between said soft layer and said bonding layer.

4. The process according to Claim 2 or 3, wherein said soft layer (11) is of a material chosen from among aluminium, aluminium and copper alloy, copper, and nickel, and said bonding layer (12) is of a material chosen from between palladium and platinum.

5. The process according to Claim 3, wherein said diffusion barrier layer (14) is of a material chosen from between chromium and titanium.

6. The process according to any of Claims 1 to 5, further comprising the step of forming spacing regions (25') having a first depth, said bonding structure comprising bonding regions (32) having a second depth greater than said first depth, wherein said pressing step comprises bringing said second substrate (34) in abutment against said spacing regions.

7. The process according to Claim 6, wherein said step of forming bonding structures comprises depositing and defining a spacing layer (25) on top of said first substrate (33) to form said spacing regions; depositing a sacrificial layer (28) on top of said first substrate and said spacing regions; selectively removing said sacrificial layer in areas to be bonded; forming a stack of layers (30, 31) including a soft layer and a bonding layer; defining said stack of layers to form said bonding regions (32) in said areas to be bonded; and removing said sacrificial layer.

8. An integrated device comprising at least one first substrate (10, 33) and at least one second substrate (13, 34), distinct from each other, and bonding structures (35) arranged between said first and said second substrate,

characterized in that said bonding structures (35) comprise portions (30) of deformed material and portions (31) of material derived from the reaction between said structures and said second substrate.

9. The device according to Claim 8, wherein said structures comprise a stack of layers including a soft layer (11) and a bonding layer (12).

10. The device according to Claim 9, further comprising a diffusion barrier layer (14) between said soft layer and said bonding layer.

11. The device according to Claim 9 or 10, wherein said soft layer (11) is of a material chosen from among aluminium, aluminium and copper alloy, copper, and nickel, and said bonding layer (12) is of a material chosen from between palladium and platinum.

12. The device according to Claim 10, wherein said diffusion barrier layer (14) is of a material chosen from between chromium and titanium.

13. The device according to any of Claims 8 to 5, further comprising spacing regions (25'; 25") having smaller deformability than said.

14. The device according to Claim 13, wherein said spacing regions (25') surround at a distance said bonding structures (35).

15. The device according to Claim 13 or Claim 14, wherein said spacing regions (25'; 25") are made of insulating material.

16. The device according to any of Claims 13 to 15, wherein said spacing regions are made of silicon dioxide.

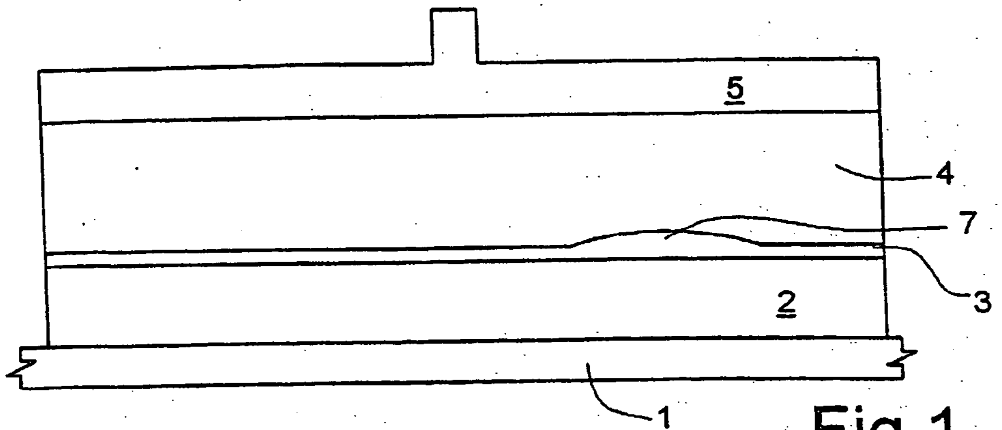

Fig.1

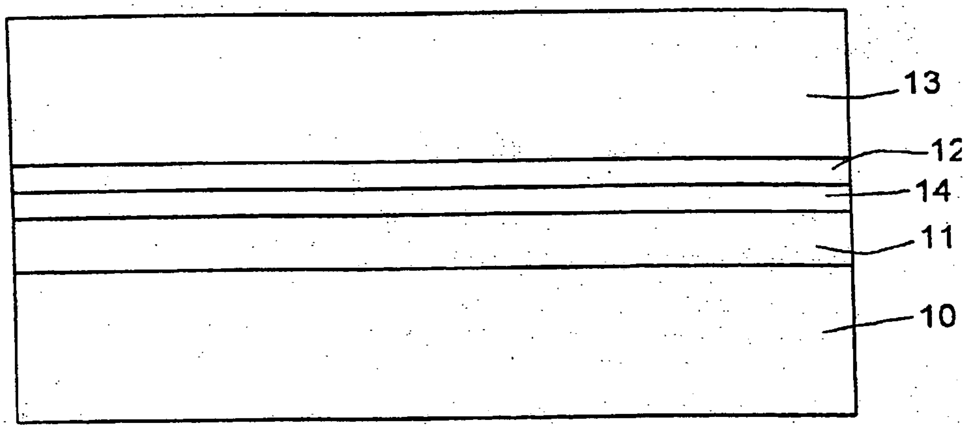

Fig.2

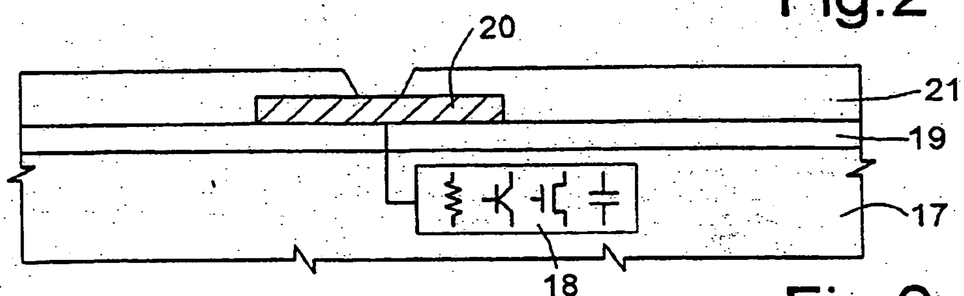

Fig.3

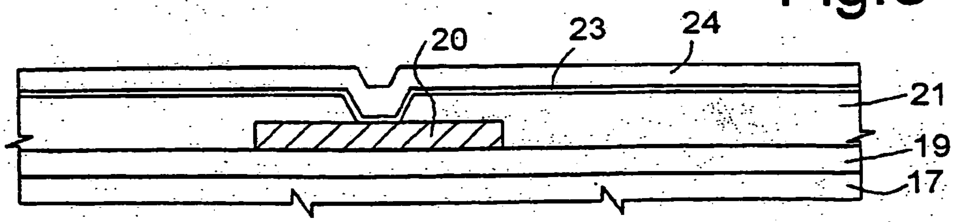

Fig.4

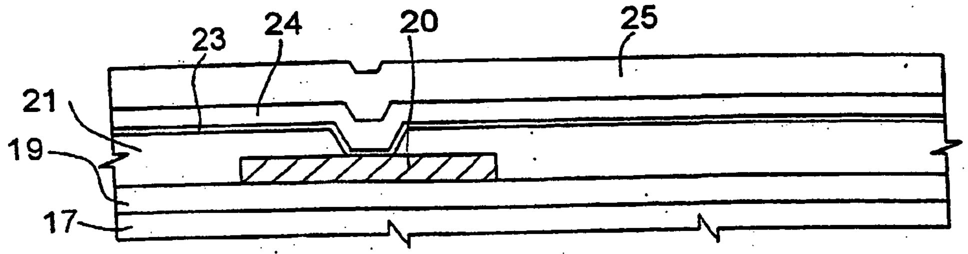

Fig.5

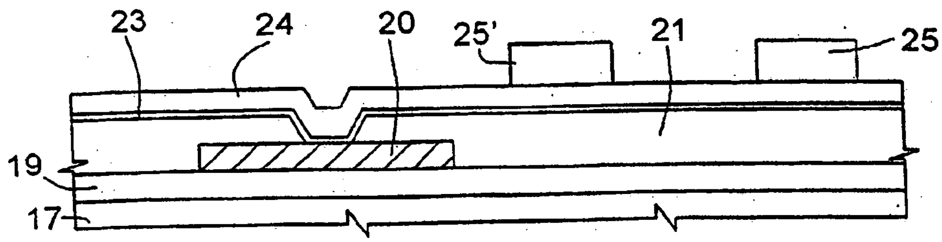

Fig.6

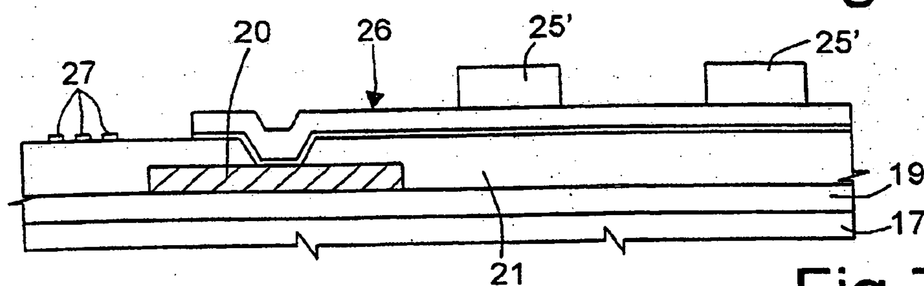

Fig.7

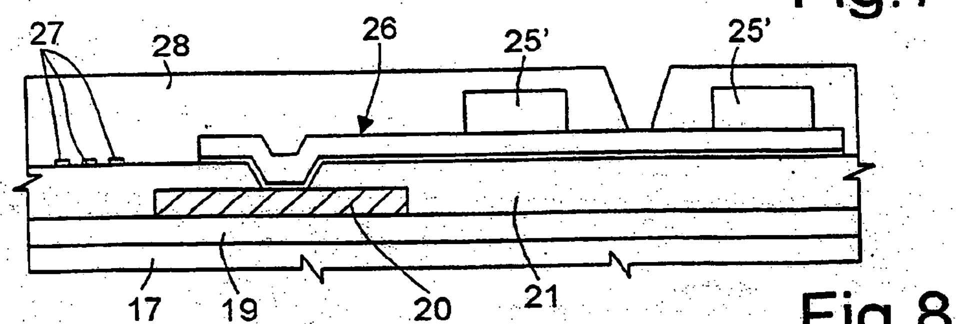

Fig.8

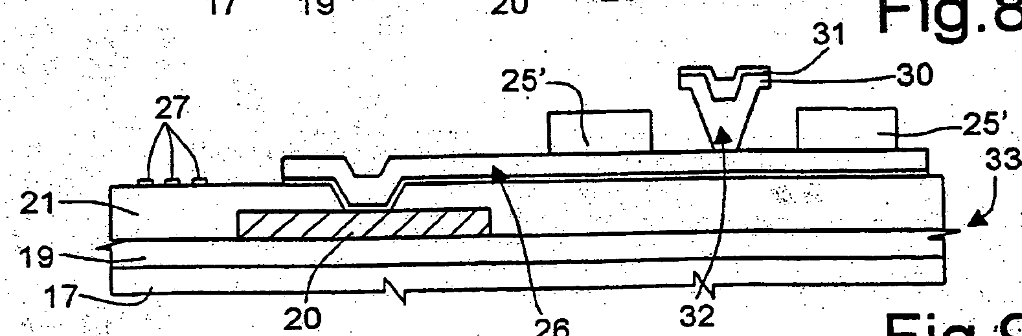

Fig.9

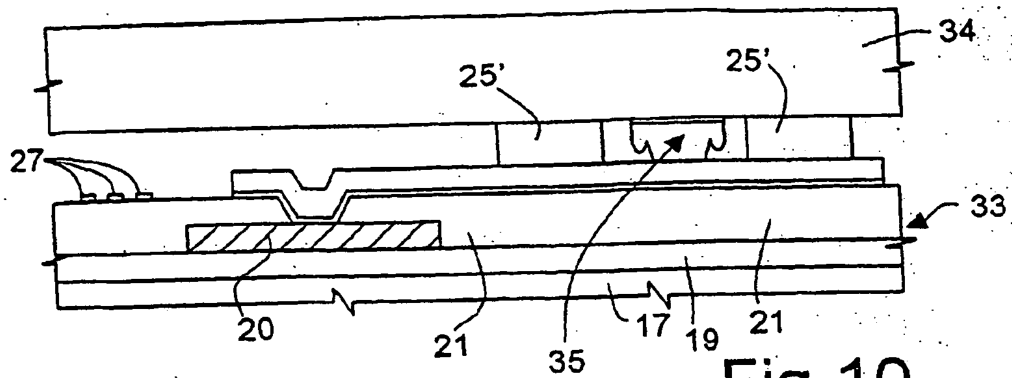

Fig. 10

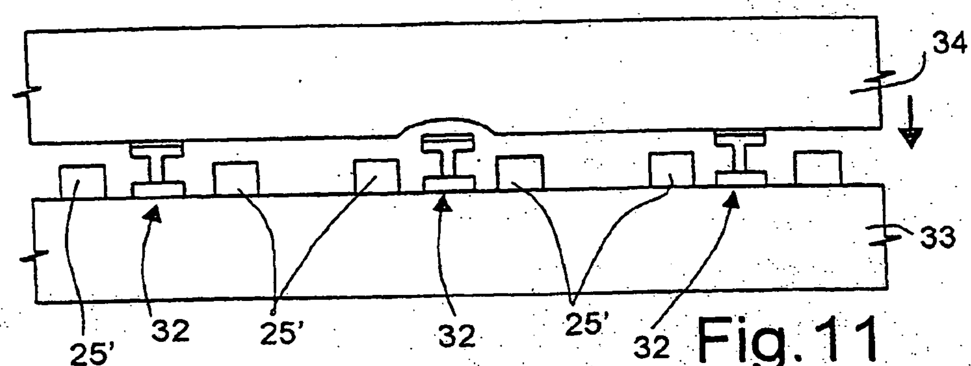

Fig. 11

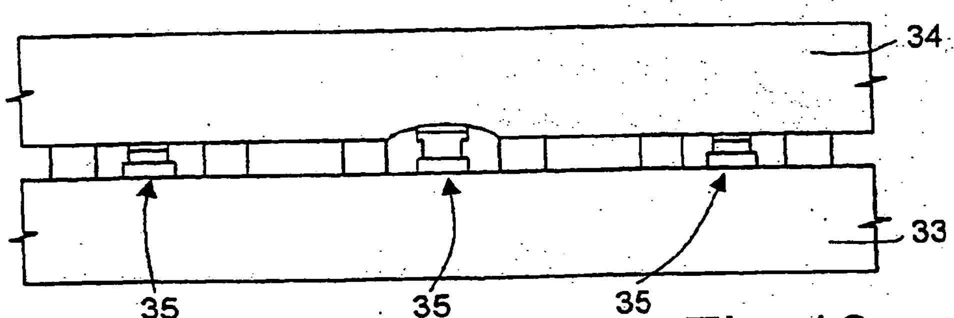

Fig. 12

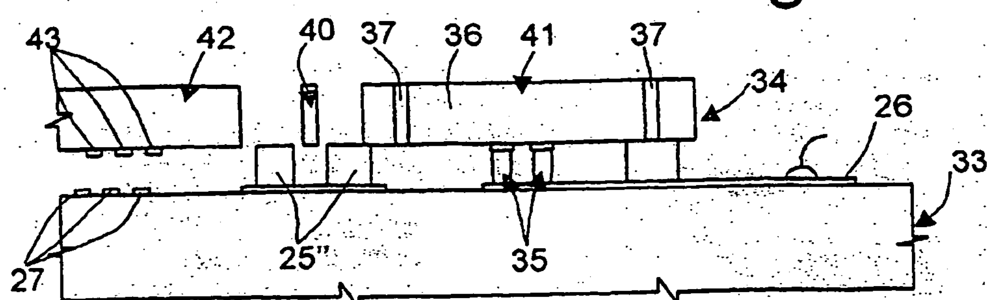

Fig. 13

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	20 February 2002	Polesello, P

CATEGORY OF CITED DOCUMENTS

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